IN THE CLAIMS

1. (Original) A semiconductor integrated circuit formed on a single semiconductor chip, comprising:

a test mode input terminal supplied with a test mode signal;

a transmitting circuit having a function of converting first parallel signals for a plurality of channels to a first serial signal;

a receiving circuit having a function of converting a second serial signal to second parallel signals for a plurality of channels;

a test signal generating circuit responsive to said test mode signal, for generating test parallel signals to be supplied to said transmitting circuit;

a first selector for supplying either said test parallel signals generated by said test signal generating circuit or said first parallel signals to said transmitting circuit;

a second selector responsive to said test mode signal, for supplying either said first serial signal supplied from said transmitting circuit or said second serial signal to said receiving circuit; and

an operation judging circuit responsive to said test mode signal, said operation judging circuit being connected so as to receive response parallel signals from said receiving

circuit,

wherein each of said test parallel signals includes a pulse sequence, and each of said response parallel signals includes a pulse sequence,

wherein said test signal generating circuit comprises a first circuit for generating test parallel signals that are equivalent to said first parallel signals for a plurality of channels, and

wherein said operation judging circuit comprises: a plurality of second circuits each capable of holding a value of one pulse in its associated one of the pulse sequences of said response parallel signals received from said receiving circuit; a plurality of third circuits for generating expected values for pulses of pulse sequences in the response parallel signals received from said receiving circuit after the pulses whose signal values have been held, based on signal values held in said second circuits; and a plurality of fourth circuits for comparing values of pulses of the pulse sequences in the response parallel signals received from said receiving circuit with the expected values generated by said third circuits.

2. (Original) A semiconductor integrated circuit according to claim 1, wherein when said test parallel signals constitute such a multi-bit signal that each pulse of a pulse

sequence in each of the test parallel signals forms one bit, said first circuit comprises:

a plurality of first flip-flop circuits for sending out said multi-bit test parallel signals;

a plurality of second flip-flop circuits disposed in a stage preceding that of said first flip-flop circuits; and

a plurality of exclusive OR circuits each for comparing values of two bits located at a distance of a predetermined number of bits between and included in bits of the test parallel signals supplied from said plurality of first flip-flop circuits, and supplying a result of the comparison to corresponding one of said plurality of first flip-flop circuits.

3. (Original) A semiconductor integrated circuit according to claim 2, wherein said operation judging circuit comprises an AND circuit for performing an AND-ing function on outputs of exclusive NOR circuits of said plurality of fourth circuits.

4. (Original) A semiconductor integrated circuit according to claim 2, wherein said operation judging circuit comprises:

an AND circuit for performing an AND-ing function on outputs of exclusive NOR circuits of said plurality of fourth

circuits;

a third flip-flop circuit for taking in an output of said AND circuit in synchronism with a clock signal; and

an SR latch circuit that is set by an output of said third flip-flop circuit.

5. (Original) A semiconductor integrated circuit according to claim 2, wherein said operation judging circuit comprises:

an AND circuit for performing an AND-ing function on outputs of exclusive NOR circuits of said plurality of fourth circuits;

a third flip-flop circuit for taking in an output of said AND circuit in synchronism with a clock signal;

an SR latch circuit that is set by an output of said third flip-flop circuit; and

a reset circuit for canceling a reset state of said SR latch circuit upon elapse of a predetermined time after a circuit disposed in a stage preceding that of said SR latch circuit is reset.

6. (Original) A semiconductor integrated circuit according to claim 1, wherein said test signal generating circuit and said operation judging circuit are formed so as to operate in accordance with a clock having a frequency

corresponding to a transfer rate of said first or second parallel signals.

Amendments to the Drawings:

The attached four replacement sheets of formal drawings include changes to FIGS. 1, 4, 5, and 6. These sheets replace the original drawing sheets having FIGS. 1, 4, 5, and 6.

In FIG. 1, the direction of the arrow for "Transmission Side Input Data" has been reversed to point toward "Transmitting Circuit", as recommended in the Office Action.

In FIG. 4, the direction of the arrow for "Reception Side Output Data" has been reversed to point toward "Operation Judging Apparatus", and the direction of the arrow for "Reception Side Input Data" has been reversed to point toward "Receiving Circuit" as recommended in the Office Action. It is noted that the Office action at Page 2, Section 2, refers to these corrections as applying to FIG. 2, rather than FIG. 4, but as FIG. 2 does not contain such arrows, and FIG. 4 was in need of such correction, the correction has been applied to FIG. 4 in response to the Office Action. If the Office Action was referring to necessary corrections other than those made in this Reply, the Examiner is urged to contact the undersigned by telephone so that corrected drawings can be submitted in a supplemental amendment.

In FIGS. 4, 5, and 6, the legend "Prior Art" has been added beneath each of the figure number designations to show that these figures illustrate the state of the prior art, as recommended by the Office Action.

Because of the minor nature of the changes to the drawings it is believed that inclusion of additional annotated sheets showing the changes in redline is not required with this Reply.

Attachments: Replacement Sheets for FIGS. 1, 4, 5, and 6